Average gate power dissipation (T_j=125)	$P_{G(AV)}$	0.5	W
Peak gate power	P		

ORDERING INFORMATION

J ST 04 G -800 SWD 6

FIG.1: Maximum power dissipation versus RMS on-state current

FIG.2: RMS on-state current versus case temperature

FIG.7: Relative variations of gate trigger current, holding current and latching current versus junction temperature

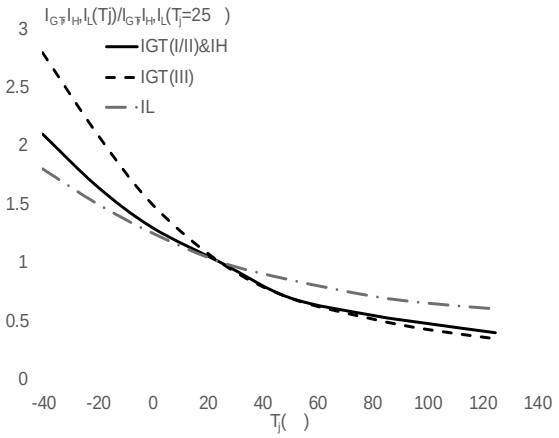
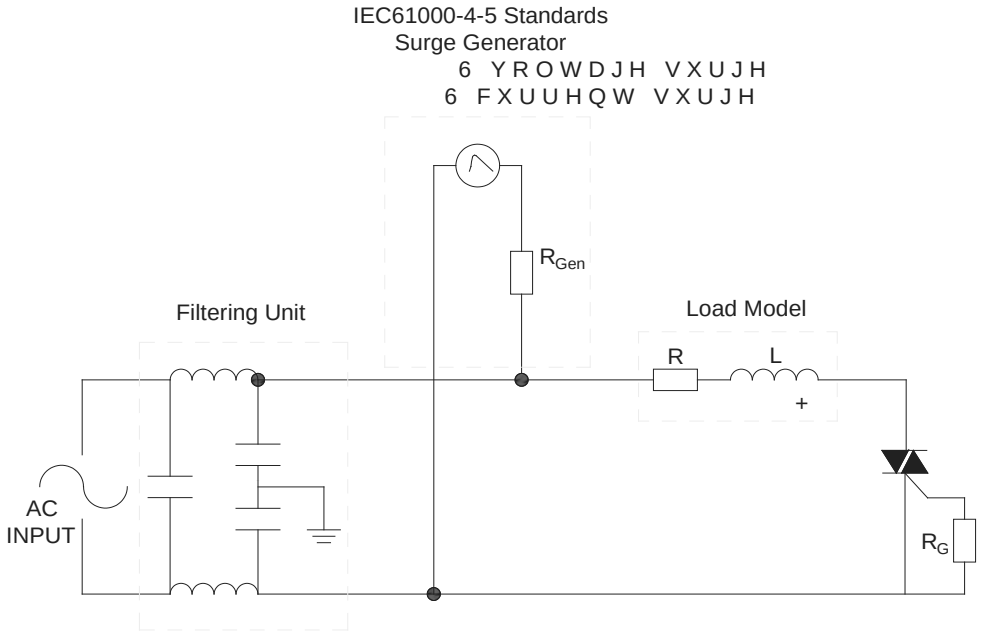


FIG.8 ÖTest circuit for inductive and resistive loads to IEC-61000-4-5 standards



ORDERING INFORMATION

Order code	Voltage V_{DRM}/V_{RRM} (V)	IGT(mA)	Package	Base qty. (pcs)	Delivery mode
		- -			

PACKAGE MECHANICAL DATA

DELIVERY MODE

PACKAGE	OUTLINE	REEL (PCS)	PER CARTON (PCS)	