JST136

ELECTRICA

Symbol		
I_{GT}		
V_{GT}		
V_{GD}		
I_L		
I_H		
dV/dt	V_D=540V Gate Open T_j=110	MIN.

E:$I_{GT1-3} \leq 10mA$ I_{GT4}

$_{RRM} \geq 800V$

FIG.1: Maximum power dissipation versus RMS on-state current

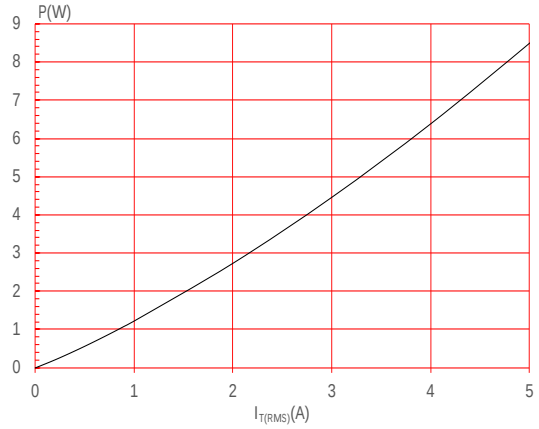


FIG.2: RMS on-state current versus case temperature

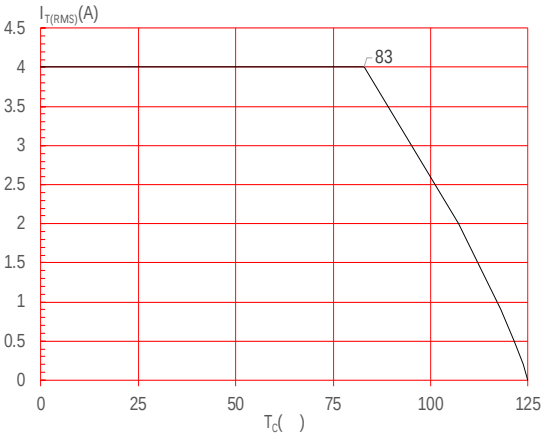
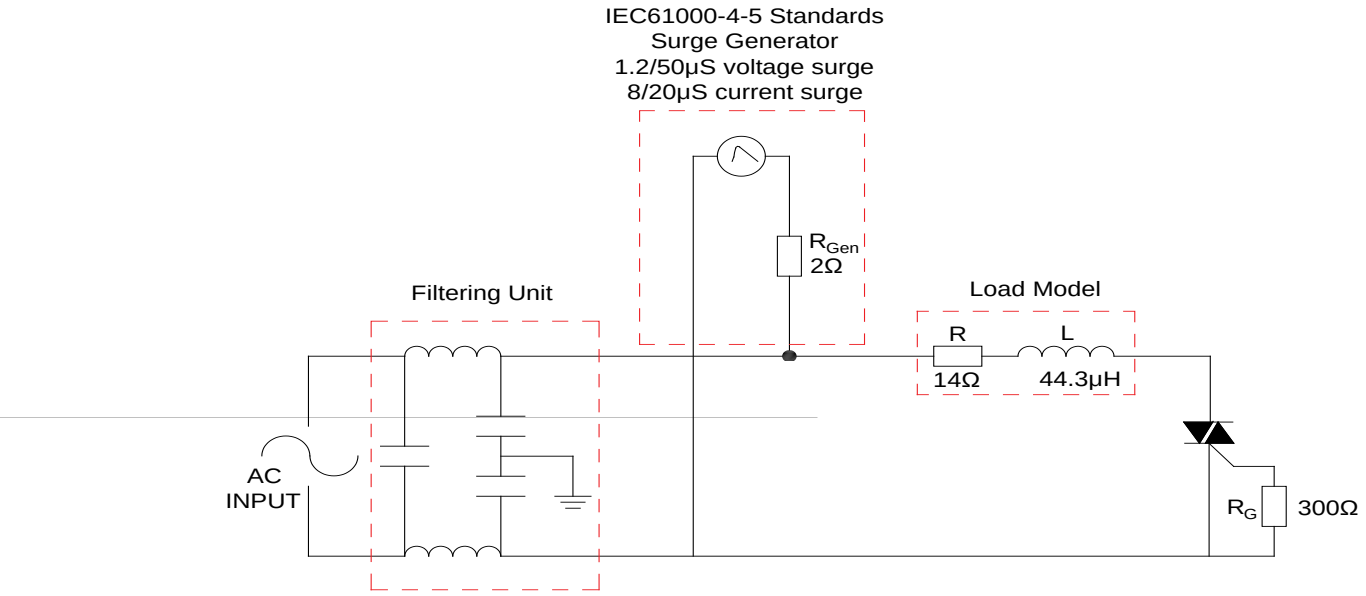


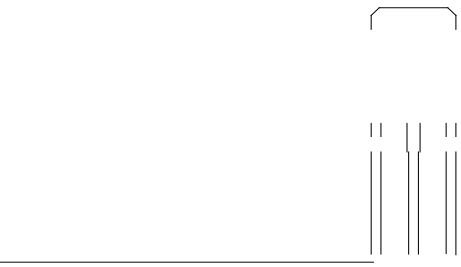
FIG.3: Surge peak on-state current versus number of cycles

FIG.4: On-state characteristics

FIG.7 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



PACKAGE MECHANICAL DATA



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co., Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it. Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.
Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information. This document supersedes and replaces all information previously supplied.

is a registered trademark of Jiangsu JieJie Microelectronics Co., Ltd.

Copyright © 2025 Jiangsu JieJie Microelectronics Co., Ltd. All rights reserved.